SYSTEM AND METHOD FOR SETTING A CLOCK RATE OF A MEMORY CARD

The Field of the Invention

[0001] The present invention generally relates to memory cards, and more particularly to a system and method for setting a clock rate of a memory card.

Background of the Invention

[0002] Many electronic devices such as digital cameras, personal and laptop computer systems, personal digital assistants (PDA), televisions, and audio and / or video media players are configured to store information to and retrieve information from memory cards that are detachable from the devices. These memory cards offer users the ability to store and transfer information between various devices by storing information from one device onto a memory card and transferring the information from the memory card to another device. For example, a user may take pictures using a digital camera that stores the pictures on a memory card. The user may then couple the memory card to a computer system to transfer the pictures from the memory card to the computer system.

[0003] Memory cards, like all electronic devices, consume electrical power in operation. The amount of power consumed by a memory card may vary with an internal clock rate of the memory card. In other words, faster clock rates may generally cause more power to be consumed by the memory card than slower clock rates. Although faster clock rates may enhance the performance of the memory card by allowing it to transfer information to and from the host device at a faster rate, the host device may not need such enhanced performance at various times. At these times, relatively slower performance produced as a result of a relatively slower clock rate may be sufficient to meet the needs of the host device.

[0004] In addition, different types of host devices may place different performance requirements on a memory card. For example, one type of device

that uses a particular memory card may require higher performance from the memory card than another type of device that uses the memory card.

Summary of the Invention

[0005] The present disclosure provides a memory card that includes a buffer configured to receive transactions, a storage media, and a control circuit coupled to the buffer and the storage media. The control circuit is configured to cause a clock signal to be provided to the buffer and the storage media at a clock rate that varies in dependence on a detected rate of the transactions received by the buffer.

Brief Description of the Drawings

[0006] Figure 1 is block diagram illustrating an embodiment of a system for setting a clock rate of a memory card.

[0007] Figure 2 is a flow chart illustrating an embodiment of a method for setting a clock rate of a memory card.

[0008] Figure 3 is a diagram illustrating an embodiment of a system that includes a memory card configured to set a clock rate.

Detailed Description

[0009] Embodiments of the invention are better understood with reference to the following drawings. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

[0010] Figure 1 is a block diagram illustrating an embodiment of a system 100 for setting a clock rate of a memory card 120 that is coupled to a host device 110, e.g., a digital camera, a personal or laptop computer system, a personal digital assistant (PDA), a television, or an audio and / or video media player such as an MP3 player. The clock rate of memory card 120 may be set to a rate that corresponds with a rate of transactions between memory card 120 and host device 110 as described in additional detail herein below.

[0011] Memory card 120 may be any type of memory card such as a CompactFlash™ memory card, a MultiMediaCard™ memory card, a Secure Digital memory card, or a Memory Stick™ memory card. Memory card 120 may be detached or removed from host device 110 and used with other host devices.

[0012] As shown, memory card 120 includes a card controller 130 and storage media 150. Card controller 130 includes a host interface 132, a processor system 134, a buffer and buffer management circuit 136, a clock control circuit 138, a master clock 140, and a media interface 142. Storage media 150 includes at least one storage medium configured to store information and may include any type or combination of non-volatile electrical, magnetic, or optical storage media such as flash memory, magnetic RAM (MRAM), atomic resolution storage (ARS), or magnetic or optical disks. The components within card controller 130 may each include hardware, software, or a combination of hardware and software.

[0013] In operation, host device 110 provides transactions such as read and write transactions, data associated with the transactions, commands, a host clock signal, and other information to memory card 120 using a bus 112. The transactions, data, commands, host clock signal, and other information are received using host interface 132. The transactions and data associated with the transactions are stored into the buffer in the buffer and buffer management circuit 136 using data lines 152 and host clock line 154. Processor system 134 provides control signals to and receives information from host interface 132 using host interface lines 156. Processor system 134 also provides control signals to and receives information from the buffer using buffer control lines 160. Buffer and buffer management circuit 136 provides buffer empty / buffer full signals to processor system 134 using one or more lines 158. In response to control signals from processor system 134, buffer and buffer management circuit 136 provides transactions and data to media interface 142 using data lines 162. Media interface 142 provides the data and media control signals to storage media 150 using data lines 166 and control lines 168, respectively. Processor system

134 provides control signals to and receives information from media interface 142 using media interface control lines 164.

[0014] In response to a write transaction from host device 110, host interface 132 stores the write transaction and the data to be stored in the buffer in buffer and buffer management circuit 136. In response to signals from processor system 134, the buffer management circuit provides the write transaction and the data from the buffer to media interface 142. Media interface 142 causes the data to be stored in storage media 150.

[0015] In response to a read transaction from host device 110, host interface 132 stores the read transaction in the buffer in buffer and buffer management circuit 136. In response to signals from processor system 134, the buffer management circuit provides the read transaction from the buffer to media interface 142. Media interface 142 causes data to be read from storage media 150 and stored in the buffer. The buffer management circuit and / or processor system 134 cause the data to be transferred from the buffer to host device 110 using host interface 132.

[0016] Master clock 140 generates a master clock signal, CLMM, at a master clock rate and provides the master clock signal CLMM to processor system 134 and clock control circuit 138. Processor system 134 provides control signals to clock control circuit 138 using a media clock control line 174. Clock control circuit 138 provides a media clock signal, CLKm, at a media clock rate to buffer and buffer management circuit 136, media interface 142, and storage media 150 using lines 172. Clock control circuit 138 also provides a processor clock signal to processor system 134 using a line 176. As described in detail below, processor system 134 may cause the media clock rate and / or the processor clock rate to be set at the same rate or a different rate as the master clock rate.

[0017] In operation, memory card 120 consumes an amount of power that may vary directly with the media clock rate of media clock signal CLKm. In other words, memory card 120 may consume more power in response to the media clock rate being set to a relatively high or fast rate and less power in response to the media clock rate being set to a relatively low or slower rate. It may be

generally desirable to minimize the amount of power consumed by memory card 120.

[0018] The functions of memory card 120 include storing data received from host device 110 and providing data to host device 110 in response to a request from host device 110. The rate at which host device 110 may call upon memory card 120 to perform these functions may vary over time. In addition, memory card 120 may be configured to operate with different types of host devices 110. Host device 110 may be a digital camera, a personal or laptop computer system, a personal digital assistant (PDA), a television, or an audio and / or video media player such as an MP3 player, for example. The rates at which different types of host devices 110 may call upon memory card 120 to perform these functions may vary. For example, a digital camera may interact with memory card 120 at different rates than an MP3 player.

[0019] Accordingly, as described in additional detail below, memory card 120 is configured to determine a rate of transactions to and / or from host device 110 and to set the media clock rate of the media clock signal CLKm in response to the rate of transactions in order to minimize the amount of power consumed by memory card 120 while ensuring that memory card 120 performs at a rate suitable for a particular host device 110.

[0020] The operation of memory card 120 will now be described with reference to Figures 1 and 2. As shown in Figure 2, the media clock signal CLKm on memory card 120 is set to a default clock rate by clock control circuit 138 as indicated in a block 202. The default clock rate may be a rate programmed by the manufacturer of the card and may be set in response to memory card 120 being powered up or reset. Alternatively, the default rate may be the rate at which memory card 120 was previously operating, i.e. prior to memory card 120 being powered down or reset.

[0021] A rate of transactions associated with memory card 120 is determined as indicated in a block 204. The rate of transactions includes a number of transactions received by memory card 120 from host device 110 over a time period. The transactions may include read transactions configured to cause information to be read from storage media 150 and provided to host device 110

and / or write transactions configured to cause information to be received from host device 110 and written to storage media 150.

[0022] In the embodiment of Figure 1, processor system 134 determines the rate of transactions by detecting a number of transactions received by buffer and buffer management 136 over one or more time periods. Processor system 134 may perform this function in various ways. For example, processor system 134 may determine the rate of transactions by monitoring how quickly the buffer in buffer and buffer management 136 fills and empties. To do so, processor system 134 monitors the number of times that it receives a buffer full signal and / or buffer empty signal from buffer and buffer management 136 over one or more time periods. Buffer and buffer management 136 generates the buffer full signal to indicate that the buffer is full and generates the buffer empty signal to indicate that the buffer is empty.

[0023] In addition, processor system 134 may determine the rate of transactions by comparing how full or empty the buffer in buffer and buffer management 136 is relative to one or more threshold values. If, for example, during a write transaction, the buffer is fuller than a high threshold, such as more than 80% full, then data is being input to the buffer faster than it is being written to storage media 150 and processor system 134 causes the clock rate of the media clock to increase. Similarly, if the buffer is less full than a low threshold, such as less than 20% full, during a write transaction, then data is being input to the buffer slower than it is being written to storage media 150 and processor system 134 causes the clock rate of the media clock to decrease. During a read transaction, processor system 134 causes the clock rate of the media clock to increase in response to determining that the buffer is less full than a low threshold, such as less than 20% full, which indicates that data is being output from the buffer faster than it is being read from storage media 150. Similarly, processor system 134 causes the clock rate of the media clock to decrease during a read transaction in response to determining that the buffer is fuller than a high threshold, such as more than 80% full, which indicates that data is being read faster from storage media 150 than it is being transferred to host device 110.

[0024] Alternatively, processor system 134 may simply count the transactions received by memory card 120 by monitoring host interface 132, buffer and buffer management 136, and / or media interface 142 over one or more time periods to determine the rate of transactions. In each of these embodiments, the rate of transactions may be associated with the number of read transactions, the number of write transactions, or the total of the number of read transactions and the number of write transactions received by memory card 120 over one or more time periods. In other embodiments, the rate of transactions of memory card 120 may be determined in other ways.

[0025] The media clock of memory card 120 is set to a clock rate associated with the rate of transactions as indicated in a block 206. In response to determining the rate of transactions, processor system 134 provides a control signal to clock control circuit 138 using media clock control line 174 to cause clock control circuit 138 to set the clock rate of the media clock. Clock control circuit 138 receives the master clock signal from master clock 140 on lines 170 and generates the media clock signal using the master clock signal. Clock control circuit 138 may generate the media clock signal at the same clock rate as the master clock signal or at a different clock rate. Clock control circuit 138 causes the media clock to be provided to the buffer in buffer and buffer management 136, media interface 142, and storage media 150 at the set clock rate. Clock control circuit 138 may also set the processor clock rate at a rate associated with the control signal.

[0026] The clock rate may vary directly with the rate of transactions. For example, in response to the rate of transactions being relatively high, the clock rate may set to a relatively high rate. Similarly, the clock rate may be set to a relatively low rate in response to the rate of transactions being relatively low. In this way, memory card 120 may be configured to process transactions at a rate that matches approximately the rate at which the transactions are received from host device 110.

[0027] Processor system 134 may determine the clock rate to be associated with the rate of transactions in various ways. For example, processor system 134 may actively and continuously monitor the empty and / or fill rates of the buffer in

buffer and buffer management 136 and incrementally increase or decrease the clock rate until the transactions are processed at a desired rate. As another example, processor system 134 may include a table that lists media clock rates for each possible range of transaction rates such that processor system 134 selects the media clock rate associated with the detected rate of transactions from the table.

[0028] In other embodiments of the method shown in Figure 2, the method may continuously repeat the functions illustrated in blocks 204 and 206. For example, subsequent to setting the media clock rate in block 206, memory card 120 may determine another rate of transactions associated with memory card 120 as indicated in block 204 and set the media clock to a clock rate associated with this other rate of transactions as indicated in block 206. In this way, memory card 120 may dynamically monitor the rate of transactions and continuously adjust the clock rate of the media clock to ensure operation at a rate suitable for host device 110.

[0029] Figure 3 is a diagram illustrating an embodiment of a system 300 that includes memory card 120 which configured to set a clock rate according to the rate of transactions received by memory card 120. In Figure 3, memory card 120 is used in conjunction with a digital camera 310. Memory card 120 detachably couples to a slot 320 of digital camera 310.

[0030] Digital camera 310 illustrates one example of a host device 110 that is configured to operate with memory card 120 as described above with reference to the embodiments of Figures 1 and 2. In particular, digital camera 310 captures image data and stores the image data onto memory card 120. In addition, digital camera 310 retrieves image data from memory card 120 and displays the image data to a user.

[0031] To capture and store image data, digital camera 310 captures an image using an image sensor (not shown). Digital camera 310 causes image data associated with the image to be provided memory card 120 using one or more write transactions. Referring back to Figure 1, memory card 120 receives the write transaction(s) using host interface 132 and causes the image data to be stored in the buffer in buffer and buffer management circuit 136. Processor

system 134 causes the image data to be stored in storage media 150 in response to the write transaction(s) using media interface 142.

[0032] To retrieve and display an image, digital camera 310 provides one or more read transactions to memory card 120 to cause image data associated with the image to be read. Host interface 132 receives the read transaction(s) and stores the read transaction(s) in the buffer. Processor system 134 causes the image data to be read from the storage media 150 and stored in the buffer in response to the read transaction(s) using media interface 142. The buffer management circuit and / or processor system 134 cause the image data to be transferred from the buffer to digital camera 310 using host interface 132. Digital camera 310 displays the image in response to receiving the image data.

[0033] In operation with digital camera 310, memory card 120 adjusts the media clock rate of the media clock signal CLKm in the manner described above with reference to Figures 1 and 2.